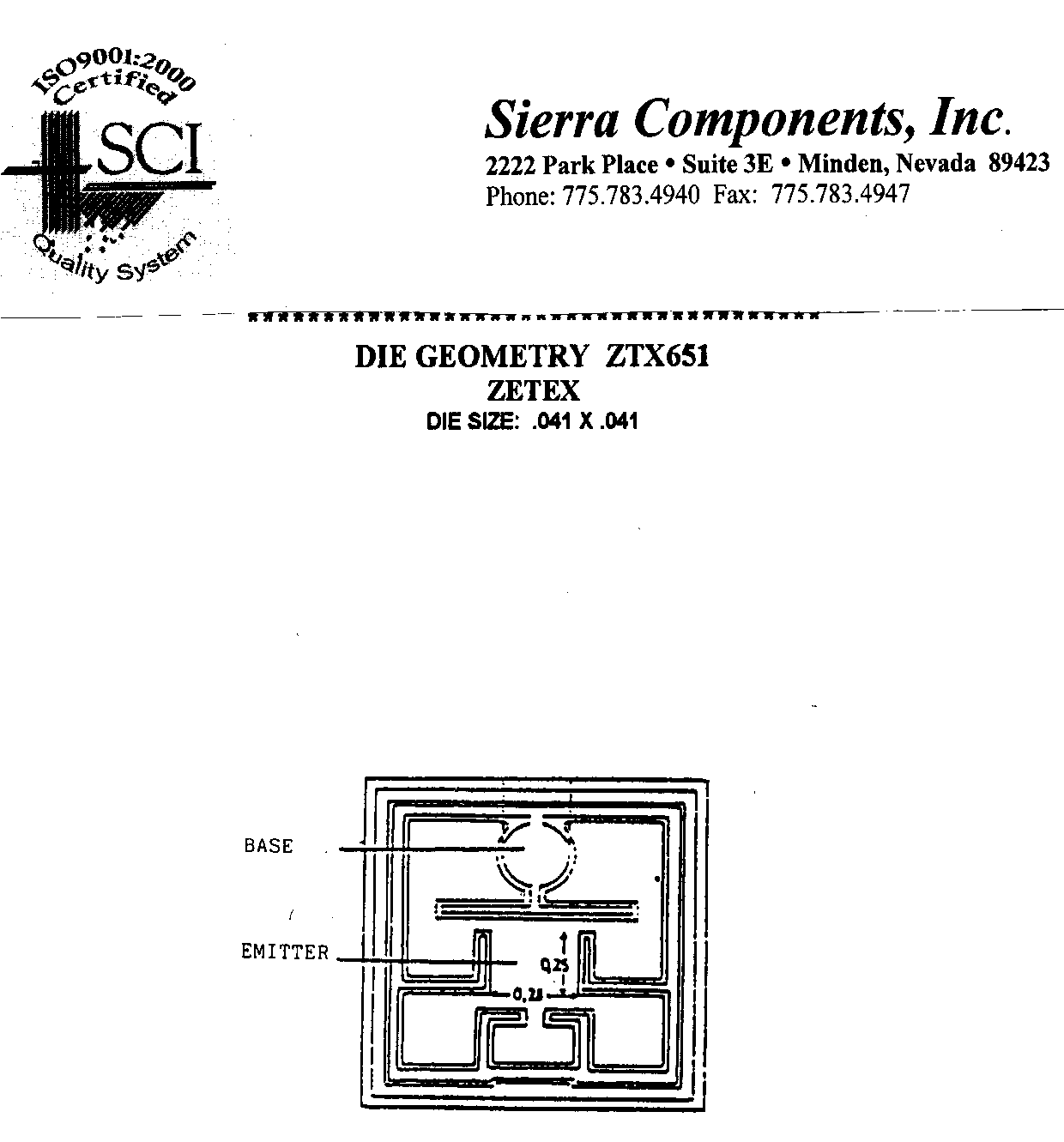
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.129”**

**PAD FUNCTIONS:**

1. **V IN (2 bond pads)**
2. **V OUT (2 bond pads)**
3. **V OUT SENSE**
4. **ADJUST**



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .025 x .025”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .041” X .041” DATE: 10/19/21**

**MFG: ZETEX THICKNESS .000” P/N: ZTX651**

**DG 10.1.2**

#### Rev B, 7/1